CLAIMS

What is claimed is:

1. A flexible and dynamically reconfigurable convolutional interleaver/de-interleaver that is operable to interleave/de-interleave a plurality of symbols, the interleaver/de-interleaver comprising:

an interleaver;

a de-interleaver that is communicatively coupled to the interleaver via a data channel;

wherein each of the interleaver and the de-interleaver includes a corresponding memory cell array, operable to store symbols therein, that includes a plurality of memory cells functionally operable to support a substantially triangular memory configuration to include a plurality of interleaver/de-interleaver array rows such that each memory cell of the memory cell array may be referenced by a row and a row position;

wherein each of the corresponding memory cell arrays is characterized by a memory block length and an interleave depth;

wherein each of the interleaver and the de-interleaver includes a corresponding write commutator, operable to communicatively couple to any interleaver/de-interleaver array row of the plurality of interleaver/de-interleaver array rows, that is operable to write a symbol to a memory cell of the memory cell array at a first time;

wherein each of the interleaver and the de-interleaver includes a corresponding first row position pointer that synchronizes with its corresponding write commutator to select the memory cell by referencing the row and the row position of the memory cell when the write commutator performs a write operation;

wherein each of the interleaver and the de-interleaver includes a corresponding read commutator, operable to communicatively couple to any interleaver/de-interleaver array row of the plurality of interleaver/de-interleaver array rows, that is operable to read the symbol from the memory cell of the memory cell array at a second time;

wherein each of the interleaver and the de-interleaver includes a corresponding second row position pointer that synchronizes with its corresponding read commutator

to select the memory cell by referencing the row and the row position of the memory cell when the read commutator performs a read operation;

wherein at least one of the first row position pointer, the interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the interleaver array row to which the read commutator communicatively couples is updated by incrementing it by a positive valued integer;

wherein the positive valued integer multiplied by the interleave depth and multiplied by a modulo function of the memory block length results in a constant value;

wherein a difference between the first time and the second time is a predetermined selectable delay that corresponds to a preselected number of symbols to be interleaved/de-interleaved by the interleaver/de-interleaver in its particular configuration; and

wherein the particular configuration of the interleaver/de-interleaver is selected from among a predetermined plurality of configurations in which the interleaver/de-interleaver may be configured.

2. The interleaver/de-interleaver of claim 1, wherein:

the first row position pointer and the interleaver/de-interleaver array row to which the write commutator communicatively couples are updated after the write commutator performs the write operation; and

the second row position pointer and the interleaver/de-interleaver array row to which the read commutator communicatively couples are updated after the write commutator performs the write operation.

3. The interleaver/de-interleaver of claim 1, wherein:

the first row position pointer and the interleaver/de-interleaver array row to which the write commutator communicatively couples are updated before the read commutator performs the read operation; and

the second row position pointer and the interleaver/de-interleaver array row to which the read commutator communicatively couples are updated before the read commutator performs the read operation.

4. The interleaver/de-interleaver of claim 1, wherein:

the write operation performed by the write commutator directs the updating of at least one of the first row position pointer, the interleaver/de-interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the interleaver/de-interleaver array row to which the read commutator communicatively couples.

5. The interleaver/de-interleaver of claim 1, wherein:

the interleaver/de-interleaver is implemented as a Ramsey Type II interleaver/de-interleaver.

6. A flexible and dynamically reconfigurable convolutional interleaver that is operable to interleave a plurality of symbols, the interleaver comprising:

a memory cell array, operable to store symbols therein, that includes a plurality of memory cells functionally operable to support a substantially triangular memory configuration to include a plurality of interleaver array rows such that each memory cell of the memory cell array may be referenced by a row and a row position;

wherein the memory cell array is characterized by a memory block length and an interleave depth;

a write commutator, operable to communicatively couple to any interleaver array row of the plurality of interleaver array rows, that is operable to write a symbol to a memory cell of the memory cell array at a first time;

a first row position pointer that synchronizes with the write commutator to select the memory cell by referencing the row and the row position of the memory cell when the write commutator performs a write operation;

a read commutator, operable to communicatively couple to any interleaver array row of the plurality of interleaver array rows, that is operable to read the symbol from the memory cell of the memory cell array at a second time;

a second row position pointer that synchronizes with the read commutator to select the memory cell by referencing the row and the row position of the memory cell when the read commutator performs a read operation;

wherein at least one of the first row position pointer, the interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the interleaver array row to which the read commutator communicatively couples is updated by incrementing it by a positive valued integer;

wherein the positive valued integer multiplied by the interleave depth and multiplied by a modulo function of the memory block length results in a constant value;

wherein a difference between the first time and the second time is a predetermined selectable delay that corresponds to a preselected number of symbols to be interleaved by the interleaver in its particular configuration; and

wherein the particular configuration of the interleaver is selected from among a predetermined plurality of configurations in which the interleaver may be configured.

7. The interleaver of claim 6, wherein:

the first row position pointer and the interleaver array row to which the write commutator communicatively couples are updated after the write commutator performs the write operation; and

the second row position pointer and the interleaver array row to which the read commutator communicatively couples are updated after the write commutator performs the write operation.

8. The interleaver of claim 6, wherein:

the first row position pointer and the interleaver array row to which the write commutator communicatively couples are updated before the read commutator performs the read operation; and

the second row position pointer and the interleaver array row to which the read commutator communicatively couples are updated before the read commutator performs the read operation.

9. The interleaver of claim 6, wherein:

the write operation performed by the write commutator directs the updating of at least one of the first row position pointer, the interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the interleaver array row to which the read commutator communicatively couples.

10. The interleaver of claim 6, wherein:

the interleaver is implemented as a Ramsey Type II interleaver.

11. A flexible and dynamically reconfigurable convolutional de-interleaver that is operable to de-interleave a plurality of interleaved symbols, the de-interleaver comprising:

a memory cell array, operable to store symbols therein, that includes a plurality of memory cells functionally operable to support a substantially triangular memory configuration to include a plurality of de-interleaver array rows such that each memory cell of the memory cell array may be referenced by a row and a row position;

wherein the memory cell array is characterized by a memory block length and an interleave depth;

a write commutator, operable to communicatively couple to any de-interleaver array row of the plurality of de-interleaver array rows, that is operable to write a symbol to a memory cell of the memory cell array at a first time;

a first row position pointer that synchronizes with the write commutator to select the memory cell by referencing the row and the row position of the memory cell when the write commutator performs a write operation;

a read commutator, operable to communicatively couple to any de-interleaver array row of the plurality of de-interleaver array rows, that is operable to read the symbol from the memory cell of the memory cell array at a second time;

a second row position pointer that synchronizes with the read commutator to select the memory cell by referencing the row and the row position of the memory cell when the read commutator performs a read operation;

wherein at least one of the first row position pointer, the de-interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the de-interleaver array row to which the read commutator communicatively couples is updated by incrementing it by a positive valued integer;

wherein the positive valued integer multiplied by the interleave depth and multiplied by a modulo function of the memory block length results in a constant value;

wherein a difference between the first time and the second time is a predetermined selectable delay that corresponds to a preselected number of symbols to be de-interleaved by the de-interleaver in its particular configuration; and

wherein the particular configuration of the de-interleaver is selected from among a predetermined plurality of configurations in which the de-interleaver may be configured.

12. The interleaver of claim 11, wherein:

the first row position pointer and the de-interleaver array row to which the write commutator communicatively couples are updated after the write commutator performs the write operation; and

the second row position pointer and the de-interleaver array row to which the read commutator communicatively couples are updated after the write commutator performs the write operation.

13. The de-interleaver of claim 11, wherein:

the first row position pointer and the de-interleaver array row to which the write commutator communicatively couples are updated before the read commutator performs the read operation; and

the second row position pointer and the de-interleaver array row to which the read commutator communicatively couples are updated before the read commutator performs the read operation.

14. The de-interleaver of claim 11, wherein:

the write operation performed by the write commutator directs the updating of at least one of the first row position pointer, the de-interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the de-interleaver array row to which the read commutator communicatively couples.

15. The de-interleaver of claim 11, wherein:

the de-interleaver is implemented as a Ramsey Type II de-interleaver.

16. A flexible and dynamically reconfigurable method for convolutional interleaving a plurality of symbols, the method comprising:

selecting an interleaving configuration from among a predetermined plurality of interleaving configurations;

configuring a memory cell array to interleave the plurality of symbols according to the selected interleaving configuration, wherein the memory cell array is operable to store symbols therein, wherein the memory cell array includes a plurality of memory cells functionally operable to support a substantially triangular memory configuration to include a plurality of interleaver array rows such that each memory cell of the memory cell array may be referenced by a row and a row position, wherein the memory cell array is characterized by a memory block length and an interleave depth;

writing a symbol to a memory cell of the memory cell array at a first time using a write commutator that is operable to communicatively couple to any interleaver array row of the plurality of interleaver array rows;

synchronizing a first row position pointer with the write commutator to select the memory cell by referencing the row and the row position of the memory cell when the write commutator performs a write operation;

reading the symbol from the memory cell of the memory cell array at a second time using a read commutator that is operable to communicatively couple to any interleaver array row of the plurality of interleaver array rows;

synchronizing a second row position pointer with the read commutator to select the memory cell by referencing the row and the row position of the memory cell when the read commutator performs a read operation; and

updating at least one of the first row position pointer, the interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the interleaver array row to which the read commutator communicatively couples by incrementing it by a positive valued integer, wherein the positive valued integer multiplied by the interleave depth and multiplied by a modulo function of the memory block length results in a constant value, wherein a difference between the first time and the second time is a predetermined selectable delay that corresponds to a preselected number of symbols to be interleaved by the interleaver in its particular configuration.

17. The method of claim 16, further comprising:

updating the first row position pointer and the interleaver array row to which the write commutator communicatively couples after the write commutator performs the write operation; and

updating the second row position pointer and the interleaver array row to which the read commutator communicatively couples after the write commutator performs the write operation.

18. The method of claim 16, further comprising:

updating the first row position pointer and the interleaver array row to which the write commutator communicatively couples before the read commutator performs the read operation; and

updating the second row position pointer and the interleaver array row to which the read commutator communicatively couples before the read commutator performs the read operation.

19. The method of claim 16, further comprising:

using the write operation performed by the write commutator to direct the updating of at least one of the first row position pointer, the interleaver array row to which the write commutator communicatively couples, the second row position pointer, and the interleaver array row to which the read commutator communicatively couples.

20. The method of claim 16, wherein:

the selected interleaving configuration supports Ramsey Type II interleaving.